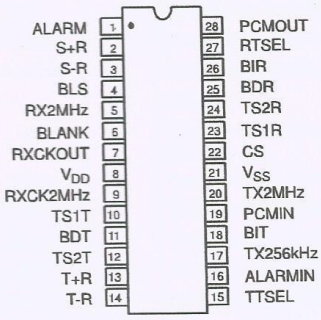
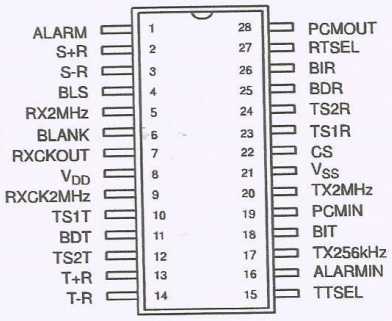
Annexure for 61/15/6137

PIN CONFIGURATION



28 Lead PDIP (0.600")



28 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	ALARM	O	**Octet Timing Alarm.** When active, indicates loss of received bipolar violations that are used for octet timing. Active high.
2	S+R	I	**Positive AMI Data to Receiver.** Positive data from the XR-T6164 receive-side. Active low.
3	S-R	I	**Negative AMI Data to Receiver.** Negative data from the XR-T6164 receive-side. Active low.
4	BLS	I	**Byte Locking Supervision.** When active, causes blanking of PCMOUT under received alarm conditions. Active low.
5	RX2MHz	I	**Receiver 2.048MHz Clock.** Used to clock out PCM data.
6	BLANK	I	**PCMOUT Data Blanking.** When active, forces PCMOUT data to all ones (AIS). Active high.
7	RXCKOUT	O	**128kHz Extracted Clock.** Clock recovered from received data.
8	V_{DD}		**+5V ±10% Power Source.**
9	RXCK2MHz	I	**2.048MHz Clock.** Used by receiver clock recovery circuit.
10	TS1T	I	**Transmitter Time-slot 1 Input.**
11	BDT	O	**Transmitter Byte Deletion Flag.** Active when a transmit byte is deleted. Active high.
12	TS2T	I	**Transmitter Time-slot 2 Input.**
13	T+R	O	**Transmit Positive AMI Data Output.** Data to XR-T6164 positive transmitter input. Active low.
14	T-R	O	**Transmit Negative AMI Data Output.** Data to XR-T6164 negative transmitter input. Active low.
15	TTSEL	I	**Transmit Time-slot Select.** When high, pin 10 is selected; when low, pin 12 is selected.
16	ALARMIN	I	**Alarm Input.** When active, inhibits insertion of violations used for octet timing in transmitter output. Active high.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Type	Description
17	TX256kHz	I	**Transmitter 256kHz Clock**. Used to output 64kbps encoded data.
18	BIT	O	**Transmitter Byte Insertion Flag.** Active when a transmit byte is repeated. Active high.
19	PCMIN	I	**Transmitter PCM Input.** Data read from the system PCM bus.
20	TX2MHz	I	**Transmitter 2.048MHz Clock.** Clocks PCM data in PCMIN.
21	V_{SS}		**Ground.**
22	CS	O	**Clock Seek.** Indicates that clock recovery circuit has loss of lock with received data. Active high.
23	TS1R	I	**Receiver Time-slot 1 Input.**
24	TS2R	I	**Receiver Time-slot 2 Input.**
25	BDR	O	**Receiver Byte Deletion Flag.** Active when received data byte is deleted. Active high.
26	BIR	O	**Receiver Byte Insertion Flag**. Active when a received data byte is repeated. Active high.
27	RTSEL	I	**Receive Time-slot Select**. When high, pin 23 is selected; when low, pin 24 is selected.
28	PCMOUT	O	**Received PCM Output Data**. Data sent to the system PCM bus.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5V ±10%, T_A = 25°C, Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Electrical Characteristics						
V_{IH}	Logic 1	2.4			V	
V_{IL}	Logic 0			0.4	V	
V_{DD}	Supply	4.5		5.5	V	
I_{DD}	Supply Current		500		µA	Dynamic Supply Current
I_{IL}	Input Leakage			1	µA	
V_{OL}				0.4	V	At 1.6mA
V_{OH}		2.4			mA	At 0.4mA
AC Electrical Characteristics						
General						
tr, tf	Output Rise/Fall Time			20	ns	All Outputs
Receiver						
tRS	RX2MHz Rising Edge to TS Rising Edge Set Up Time	0		tRXL-100	ns	*Figure 3*
tRH	RX2MHz Rising Edge to TS Falling Edge Hold Time	0		tRXL-100	ns	*Figure 3*
tDRS	TS Rising Edge to Leading Edge of PCMOUT D0 Bit Delay			10	ns	*Figure 3*
tDRH	TS Falling Edge to Trailing Edge of PCMOUT D7 Bit Hold Time	0		10	ns	*Figure 3*
tRXD	RX2MHz Rising Egde to PCMOUT Bits D1 Through D6 Rising Edge Delay			10	ns	*Figure 3*
tPW	PCMOUT Pulse Width		488		ns	*Figure 3*
tRXH	RX2MHz High Time		244		ns	*Figure 3*
tRXL	RX2MHz Low Time		244		ns	*Figure 3*
tRXCLK	RX2MHz Period		488		ns	±100ppm
Transmitter						
tTS	TS Rising Edge to TX2MHz Set Up Time	20		tTXL-100	ns	*Figure 5*
tTH	TS Falling Edge to TX2MHz Hold Time	0		tTXL-100	ns	*Figure 5*
tDS	PCMIN Edge to TX2MHz Set Up Time	100			ns	*Figure 5*
tDH	PCMIN Edge to TX2MHz Hold Time	100			ns	*Figure 5*
tTXH	TX2MHz High Time		244		ns	*Figure 5*
tTXL	TX2MHz Low Time		244		ns	*Figure 5*
tTXCLK	TX2MHz Period		488		ns	±100ppm